A 37~ 50 GHz InP HBT VCO IC for OC-768 Fiber Optic Communication Applications

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Abstract **This paper reports a 50GHz voltage-controlled-oscillator (VCO) integrated circuit (IC) designed for OC-768 fiber optic communication applications. Implemented with a 140GHz f_t InP HBT technology, the VCO IC is designed based on a modified Colpitts configuration with a unique resonator to maximize the tuning range. Tuned by a single-ended voltage, the VCO exhibits 37~50GHz (30%) tuning-range over a tuning voltage range of 1.2V.**

I. INTRODUCTION

40GHz VCO is a key component in both MUX and DEMUX for OC-768 fiber optical communication applications, especially when 20GHz in-phase (I) and quadrature (Q) local clocks are required. Traditionally, the I-Q outputs are generated (1) by using a *RC-CR* phase shifter together with power-consuming phase correction circuits [1], (2) by coupling two differential VCOs[2-5], with accuracy limited by on-chip component matching or (3) by running the LO at twice the desired frequency and using the I-Q outputs of a flip-flop frequency divider. Although VCO architectures that inherently produce I-Q components are applicable to most RF wireless applications, at OC-768 frequencies, the frequency divider architecture proves to be more attractive because of its accuracy and compactness.

With various forward-error-correction (FEC) schemes/ overheads, OC-768 data rates range from 39 to 50Gbps. It is desirable for a VCO to cover the entire range so that a single MUX/DMUX design can support all FEC schemes. It remains, however, a challenge to design such a VCO of high operating frequency, broad tuning range and relatively low phase noise. This paper reports a 37~ 50 GHz VCO for OC-768 fiber optical communication applications.

II. 50 GHz VCO CORE

LC resonator based Colpitts architecture is advantageous for the wide tuning range requirement provided that varactors are used as tuning elements. The reason lies in that Colpitts has two capacitors in its tank circuit and by design both of them can contribute to broaden the VCO tuning range.

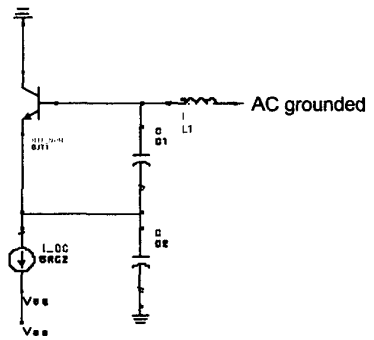

Fig.1 Single-ended Colpitts Oscillator

For VCO of Colpitts topology shown in Fig.1, the first order approximation of the oscillating frequency is given by

$$f_0 = \frac{1}{2\pi\sqrt{L_1 \dfrac{C_1 C_2}{C_1 + C_2}}} \qquad (1)$$

For 50GHz oscillations, key component L1 might range form 0.1 to 0.15nH, C_1 and C_2 from 80 to100fF. Frequency tuning could be realized by adjusting C_1 and/or C_2, implemented using varactors. Based on our InP double hetero-junction bipolar technology (DHBT), a standard varactor cell is formed with a $1x20\mu m^2$ BC junction, which provides 17fF of capacitance at zero bias and has at least 50% varying range between bias voltages of +0.3 and -0.7V. BJT_1 is single cell non-self-alignment InP HBT with $1x6\mu m^2$ emitter size The HBT has a peak 140GHz f_t and 170GHz f_{max}. Peak f_t occurs at $1mA/\mu m^2$ current density. The HBT cell has C_{bc} and C_{be} of 25fF at zero bias, which are in parallel with the variable capacitors and therefore is detrimental to tuning range of the VCO. Considerable challenges lie in minimizing the impact of parasitics, which include both component and layout parasitics.

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In addition, frequency dependence of L_1, which is usually implemented with short-ended transmission lines for 50GHz frequency operation, will also decrease the tuning range. Consider a single-ended inductor that is implemented with a homogenous transmission line having characteristic impedance Z_0 and length l. With one end grounded, the impedance at the other terminal is

$$Z = jZ_0 \tan\frac{\omega_c l\sqrt{\varepsilon_{eff}}}{c}, \qquad (2)$$

where ω_c denotes angular oscillating frequency, c free space light speed, ε_{eff} the effective dielectric constant, which is determined by the cross-section dimensions and material properties of the transmission line. For quasi-TEM mode, the frequency dependence of ε_{eff} is so weak that the resultant dispersion can be neglected below 100GHz for the on-chip transmission line dimensions. The equivalent inductance presented at the single-end port is

$$L = Z_0\frac{l\sqrt{\varepsilon_{eff}}}{c}\sec^2\frac{\omega_c l\sqrt{\varepsilon_{eff}}}{c} \qquad (3)$$

The frequency dependence of the inductance unfortunately degrades the tuning range. When the VCO frequency is tuned to higher frequency by decreasing C_1 and C_2, the inductance L_1, increases and consequently reduces the maximum operating frequency. To minimize such effect, the electrical length (l) of the transmission line $\frac{\omega_c l\sqrt{\varepsilon_{eff}}}{c}$ should be designed to be as short as possible. Reducing l lowers the Q factor and therefore degrades phase noise performance, as discussed in [5]. An excessively shrunk l may eventually stop oscillation. 5° electrical length turns out to be a good trade off.

Simplified schematic of VCO core having aforementioned features is shown in Fig.2, where CPW1 and CPW_2 provide inductance L, and $DIODE_1$ to $DIODE_4$ capacitance to form a Colpitts oscillator. The sizes of the varactors need to be maximized for largest tuning range and consequently the inductance of the CPWs need to be reduced to keep the center oscillating frequency at 43GHz. Unfortunately, excessively low inductances will result in reduction of Q factor and loop gain, hence the size of the varactors will eventually be limited by minimum loop gain and Q-factor demanded by phase noise specification. Tap ratio also will impact phase noise performance [7]. By simulation, a good tradeoff between tuning range and phase noise performance is to have 3 standard varactor cells in each of the DIODES 1~4, reflecting an optimal tap ratio of approximately 1:1.

In the layout, CPW_1 and CPW_2 were arranged into U-shaped tanks with opening at one end to accommodate transistors and varactors in the loop and form a unique resonator, where the impact of interconnects in the tank circuit are minimized. Two types were considered for CPW_1 and CPW_2, i.e. double- and single-side grounded CPWs. Single-side grounded CPW was considered superior because of high modeling accuracy, lower metal loss and higher characteristic impedance.

RFC_1, C_1 and C_2 were introduced to have all varactors biased at the same DC voltage over the whole tuning voltage range so as to maximize the effective sweep range of V_{tune}. The value of C_1 and C_2 were carefully chosen. Large size allows large tuning range, however, excessively big MIM plates will introduce large capacitive coupling to nearby ground. These capacitive parasitics decrease tuning range and also lower oscillating frequencies.

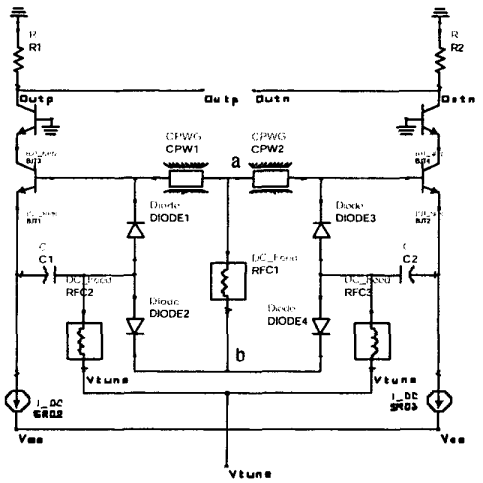

Fig.2 Differential Form of Colpitts VCO with cascode output stages

Nodes a and b were AC isolated by RFC1 and DC biased using a simple resistor voltage divider. For differential mode, nodes a and b are virtual grounds. That will relax the requirement for RFC1. Moreover, because of AC floating nodes a and b, common mode oscillation was effectively suppressed. Large varactor size also simplifies the design of RFC_2 and RFC_3, which are in parallel with $DIODE_2$ and $DIODE_4$. 200Ω resistor and 200μm/2μm microstripe formed between M1 and M2 proved to be good enough for RFC_1 through RFC_3.

SRC_2 and SRC_3 were designed capable of providing up to 6mA, the current to achieve maximum current density allowed for BJT_1 through BJT_4. When operating at 4.2V power supply voltage, simple current mirrors were used as

DC current sources SRC_2 and SRC_3. Bases of output cascode stages BJT_3 and BJT_4 were grounded to simplify the bias circuitry and maximize the V_{ce} of the core transistors BJT_1 and BJT_2. $1x12\mu m^2$ cells are used as BJT_3 and BJT_4 for lower current density operation to alleviate effect caused by low V_{ce}.

III. BUFFER DESIGN

For 50GHz operation, the buffer was designed as 3 stage cascaded emitter followers (EF) followed by a cascode different output stage, as shown in Fig. 3. The transistors are sized as $1x6\mu m^2$ in the three EF stages and $1x12\mu m^2$ in output stage. All of the transistors are operating close to highest current density. Resistors R_1 through R_6 in EF stages are designed to allow three EF stages operating close to the maximum current density. The advantage of these pull-down resistors over current sources in emitter followers is good stability. This confines the power supply voltage within a range of 4.0 to 4.4V. The overall gain and the output swing of the buffer could be adjusted by setting V_{amp} and V_{cs}. Typically, the buffer could provide a 500mV output peak-to-peak swing to an off-chip 100Ω deferential load. Emitter degeneration resistor R_9 functions to suppress the gain of the buffer at low frequencies.

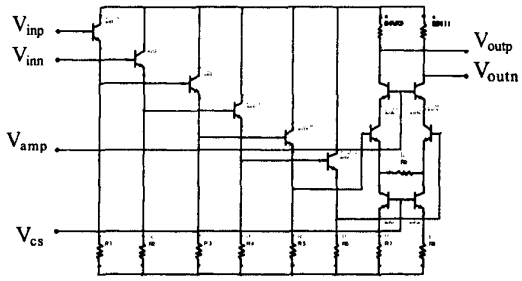

Fig.3 50GHz VCO buffer

Careful analysis shows that potential oscillation within the buffer can be avoided by shortening the input and interstage interconnects, which are implemented in microstrip form with M1 and M2 (or CPW). Decreasing cascaded EF stage numbers can alleviate instability caused by negative resistance at EF input but with degraded t swing at 50 GHz.

The buffer, drawing 35mA from a –4.2V supply, consumes much more power than the VCO core. The high power dissipation is mainly due to high current bias in the emitter follower stages for broadening the bandwidth. Moreover, the buffer can be merged with internal clock buffer when embedded into MUX or DEMUX chip, thus greatly reducing power consumption.

IV. SIMULATION

Harmonic Balance and Transient Analyses in Agilent's Advanced Design System were used to predict the oscillation frequency and phase noise of the VCO. Extensive post-layout simulations were made to factor in layout paracitics. In post-simulation, we attempted to model all paracitics in the layout, including short interconnects. Most interconnects in the layout were implemented with transmission lines for higher modeling accuracy. For interconnects far away from a ground plane, worst case parasitics were simulated to check the design robustness. Capacitive coupling between the key nodes and the ground plane were also considered in simulations.

V. CHARACTERIZATION

Figure 4 shows a microphotograph of the 50GHz VCO with a buffer integrated on a single chip. The chip measured 1000μm x 700μm. DC pads were used for ground, power, and the tuning voltage. AC output pads were designed to interface to a 150μm pitch GSGSG microwave probe.

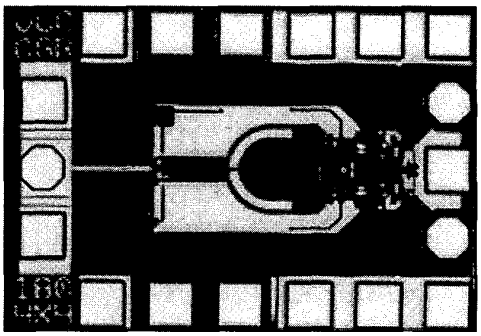

Fig.4 Microphotograph of the 50GHz VCO

Characterization set up of the VCO consists of DC probes, 50GHz GSGSG probe and an Agilent 8565E spectrum analyzer. Dc probes provide –4.2V power supply and also the tuning voltage. One output of the VCO was terminated by a 50Ω load while the other output was connected to the 8564E by a 1.5 meter 50GHz cable, which was calibrated to have 3.5dB loss at 50GHz.

Fig. 5 (a) shows the measured tuning curve of the VCO, where 37~50GHz (30%) tuning range is observed over a tuning voltage swept from –1.4 to –2.5V, corresponding to

the varactor bias of 0.3V to -0.8V. The average tuning sensitivity is greater than 10GHz/V. In Fig.5 (b), −9dBm single-ended output was observed over the entire frequency band. The output power level is equivalent to 400~500mVp-p voltage swing at a 100Ω off-chip differential load. Including the buffer power consumption, the VCO chip drew 47mA from a single −4.2V power supply. The VCO performance and power consumption were in very good agreement with simulation. It should be emphasized that the VCO core, including all bias circuits, draws only 12mA.

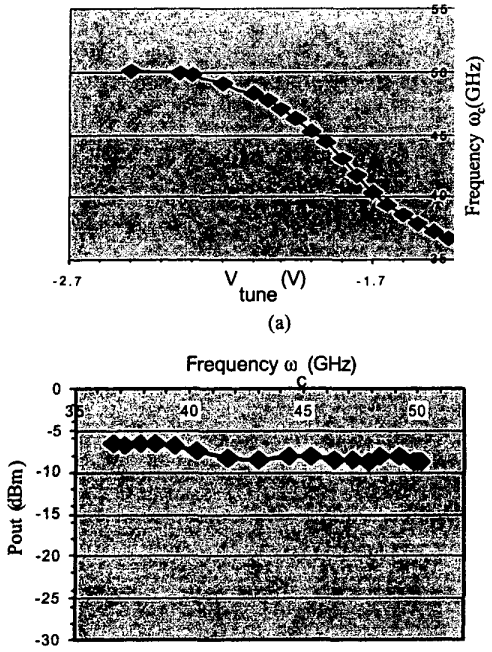

Fig. 5 Measured tuning range (a), and single-ended output power (b)

Fig. 6 Measured VCO spectrum

Fig.6 shows the measured 50GHz spectrum of the VCO operating at free running mode. −8.50dBm single-end power was observed even without accounting for the loss in the cable. Within the 0~50GHz, only one oscillation mode was found. The oscillation exhibits stable output power level and frequency. Limited by test setup, accurate phase noise measurements have not been performed. Estimated from the spectrum, the phase noise range for 98~103dBc/Hz at 10MHz offset over the whole frequency band. Again, this is very close to the phase noise predicted by frequency sensitivity analysis (pnfm) and phase noise mixing analysis (pnmx) at 10MHz frequency offset with Agilent's ADS.

We have successfully implemented a 40GHz MUX/CMU that incorporated the VCO inside and the work will be published in separate papers.

VI. CONCLUSIONS

An LC resonator based VCO covering the entire OC-768 fiber optical communication frequency band has been successfully developed based on an InP HBT technology with 140GHz f_t and 170GHz f_{max}. The VCO was characterized to have 37~50GHz (30%) tuning range over a 1.2V sweep width and deliver 6dBm to a 100Ω differential off-chip load through a buffer with excellent flatness over the whole tuning range. Powered with a single −4.2V supply, the VCO core draws a mere 12mA. Phase noise is measured to be 100dBc at 10MHz offset across the entire tuning range of the VCO.

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